



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,584	12/28/2001	Guy L. Steele JR.	06502.0366	2869

7590 10/04/2004  
Finnegan, Henderson, Farabow,  
Garrett & Dunner, L.L.P.  
1300 I Street, N.W.  
Washington, DC 20005-3315

EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/035,584	STEELE, GUY L. <i>de</i>
	<b>Examiner</b>	<b>Art Unit</b>
	Chat C. Do	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1) Responsive to communication(s) filed on 12/28/01;3/6/02;3/27/02;4/26/02;11/19/02.

2a) This action is **FINAL**.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-37 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5)  Claim(s) \_\_\_\_\_ is/are allowed.  
6)  Claim(s) 1-37 is/are rejected.  
7)  Claim(s) \_\_\_\_\_ is/are objected to.  
8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 28 December 2001 is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892) 4)  Interview Summary (PTO-413)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. \_\_\_\_.  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/6/02;11/19/02;...  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

1. The disclosure is objected to because of the following informalities:

The applicant is advised to update information cited in the “related applications” section in the present application.

Appropriate correction is required.

### ***Claim Objections***

2. Claims 8-11, 20, 22, 32, and 34 are objected to because of the following informalities:

Re claim 8, the applicant is advised to amend the phrase “a +OV status and a -OV status” in line 2 as “a plus overflow (+OV) status and a minus overflow (-OV) status” for clarification. Claims 20 and 32 have the same objection.

Re claim 9, the applicant is advised to amend this claim to depend on claim 8 because only precedence claim 8 discloses the overflow status.

Re claim 10, the applicant is advised to amend the phrase “a +UN status and a -UN status” in line 2 as “a plus underflow (+UN) status and a minus underflow (-UN) status” for clarification. Claims 22 and 34 have the same objection.

Re claim 11, the applicant is advised to amend this claim to depend on claim 10 because only precedence claim 10 discloses the underflow status.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 6, the limitation “the structure of a decision table” in line 2 lacks an antecedence basis since the structure is not mentioned in precedence claims. For examination purposes, the examiner considers the limitation as “a structure of a decision table”.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-37 are rejected under 35 U.S.C. 103(a) as being obvious over Huang et al. (U.S. 5,995,991) in view of Nakano (U.S. 5,065,352).

Re claim 1, Huang et al. disclose in Figures 1 and 4 a system (abstract) for providing a floating point product (col. 7 lines 65-66 and 114 in Figure 4), comprising: an analyzer circuit (24 and 26 in Figure 1; 116-2 and 118-2 in Figure 4; and col. 7 lines 10-17) configured to determine a first status of a first floating point operand (e.g. output of

116-2) and a second status of a second floating point operand (e.g. output of 118-2) based upon data within the first floating point operand and data within the second floating point operand respectively, and a results circuit coupled (114, 150, and 122) to the analyzer circuit (116-2 and 118-2) and configured to assert a resulting floating point operand containing an arithmetic (as multiplication and col. 7 lines 65-66) of the first floating point operand and the second floating point operand and a resulting status embedded (e.g. output of 150) within the resulting floating point operand. Huang et al. do not disclose the result is the remainder of operands. However, Nakano discloses in Figure 1 an operation to yield a remainder of two operands division (abstract lines 6-14) utilizing multiplication. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add an algorithm to determine a remainder of division utilizing a multiplication as seen in Nakano's invention into Huang et al.'s invention because it would enable to enhance the system performance and reduce the circuitry of determining the remainder of division.

Re claim 2, Huang et al. further disclose in Figures 1 and 4 the analyzer circuit further comprises: a first operand buffer (e.g. 112) configured to store the first floating point operand, a second operand buffer (e.g. 112) configured to store the second floating point operand, a first operand analysis circuit (116-2) coupled to the first operand buffer, the first operand analysis circuit configured to generate a first characteristic signal having information relating to the first status (table 1 in col. 6); and a second operand analysis circuit (118-2) coupled to the second operand buffer, the second operand analysis circuit

configured to generate a second characteristic signal having information relating to the second status (table 1 in col. 6).

Re claim 3, Huang et al. further disclose in Figures 1 and 4 the first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer (116-2 and 118-2).

Re claim 4, Huang et al. further disclose in Figures 1 and 4 the memory storage external to the first operand buffer and the second operand buffer is a floating-point status register (112 for storing the status information as example of output of 150).

Re claim 5, Huang et al. further disclose in Figures 1 and 4 the results circuit further comprises: an arithmetic circuit (114 and col. 7 lines 65-66) coupled to the analyzer circuit (116-2 and 118-2), the arithmetic circuit configured to produce the result of the first floating point operand and the second floating point operand (output of 114), a arithmetic logic circuit (150) coupled to the analyzer circuit and configured to produce the resulting status based upon the first status and the second status (150), and a result assembler coupled to the arithmetic circuit and the arithmetic logic circuit, the result assembler configured to assert the resulting floating point operand and embed the resulting status within the resulting floating point operand (112). Huang et al. do not disclose the result or the arithmetic is the remainder of operands. However, Nakano discloses in Figure 1 an operation to yield a remainder of two operands division (abstract lines 6-14) utilizing multiplication. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to add an algorithm to determine a remainder of division utilizing a multiplication as seen in

Nakano's invention into Huang et al.'s invention because it would enable to enhance the system performance and reduce the circuitry of determining the remainder of division.

Re claim 6, Huang et al. further disclose in Figures 1 and 4 the multiplier logic circuit is organized according to the structure of a decision table (table 1 in col. 6).

Re claim 7, Huang et al. further disclose in Figures 1 and 4 the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, division by zero status, an infinity status, and an inexact status (col. 7 lines 20-22).

Re claim 8, Huang et al. further disclose in Figures 1 and 4 the overflow status represents one in a group of a +OV status and a -OV status (col. 1 lines 55-60 and col. 7 lines 20-23).

Re claim 9, Huang et al. further disclose in Figures 1 and 4 the overflow status is represented as a predetermined non-infinity numerical value (table 1 in col. 6).

Re claim 10, Huang et al. further disclose in Figures 1 and 4 the underflow status represents one in a group of a +UN status and a -UN status (col. 1 lines 55-60 and col. 7 lines 20-23)..

Re claim 11, Huang et al. further disclose in Figures 1 and 4 the underflow status is represented as a predetermined non-zero numerical value (table 1 in col. 6).

Re claim 12, Huang et al. further disclose in Figures 1 and 4 the invalid status represents a not-a-number (NaN) status due to an invalid operation (col. 6 lines 39-43).

Re claim 13, Huang et al. further disclose in Figures 1 and 4 the infinity status represents one in a group of a positive infinity status and a negative infinity status (col. 9 lines 25-30).

Re claim 14, it is a method claim of claim 1. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 15, it is a method claim of claim 2. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 16, it is a method claim of claim 3. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 17; it is a method claim of claim 4. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 18, it is a method claim of claim 5. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 19, it is a method claim of claim 7. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 20, it is a method claim of claim 8. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 21, it is a method claim of claim 9. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 22 it is a method claim of claim 10. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 23, it is a method claim of claim 11. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 24, it is a method claim of claim 12. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 25, it is a method claim of claim 13. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 26, it is a computer-readable medium claim of claim 1. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 27, it is a computer-readable medium claim of claim 2. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 28, it is a computer-readable medium claim of claim 3. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 29, it is a computer-readable medium claim of claim 4. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 30, it is a computer-readable medium claim of claim 5. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 31, it is a computer-readable medium claim of claim 7. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 32, it is a computer-readable medium claim of claim 8. Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 33, it is a computer-readable medium claim of claim 9. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 34, it is a computer-readable medium claim of claim 10. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 35, it is a computer-readable medium claim of claim 11. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 36, it is a computer-readable medium claim of claim 12. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 37, it is a computer-readable medium claim of claim 13. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

### ***Double Patenting***

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-37 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of copending Application No. 10/035580 in view of Nakano (U.S. 5,065,352).

Claims 1, 5, 14, 18, 26, and 30 of the present application have same limitations cited in claim 1, 5, 15, 19, 28, and 32 of the copending Application except the present

application claims the result as the remainder of a division of two operands and the copending Application claims the result as the product of a multiplication of two operands. However, Nakano discloses in Figure 1 a multiplication is used to perform the remainder of a division or vice versa (abstract lines 7-15). Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to compute a remainder of a division using a multiplication as seen in Nakano's invention into the present application's invention because it would enable to enhance the system performance and reduce the circuitry of computing a division.

Claims 2-4, 6-13, 15-17, 19-25, 27-29, and 31-37 of the present application have exact limitations cited in claims 2-4, 6, 8-14, 16-18, 21-27, 29-31, and 34-40 of the copending Application respectively.

This is a provisional obviousness-type double patenting rejection.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 6,490,607 to Oberman discloses a shared FP and SIMD 3D multiplier.
- b. U.S. Patent No. 6,105,047 to Sharangpani et al. disclose a method and apparatus for trading performance for precision when processing denormal numbers in a computer system.

c. U.S. Patent No. 6,151,669 to Huck et al. disclose methods and apparatus for efficient control of floating-point status register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do  
Examiner  
Art Unit 2124

September 27, 2004

*recc'd. cl.*  
KAKALI CHAKI  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100